DIGITAL IMAGE PROCESSING DEVICE

BACKGROUND OF THE INVENTION

5 ### Field of the Invention

The present invention relates to a digital image processing device and more particularly to the digital image processing device to feed image data to an image display device.

10   The present application claims priority of Japanese Patent Application No.2003-090064 filed on March 28, 2003, which is hereby incorporated by reference.

Description of the Related Art

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Resolutions being employed in a digital image processing device includes, for example, in the case of a color-display plasma display panel, many levels of resolutions mainly such as WVGA (Wide-Video Graphics Array) providing 2559 pixels X 480 lines,

20 HD (High-Definition) providing 3072 pixels X 768 lines, and WXGA (Wide-Extended Graphics Array) providing 4095 pixels X 768 lines and such the resolutions tend to increase in level. To supply a display panel at a low cost, a method is employed in which, by achieving commonality of specifications of components including

25 a comparatively high-cost driving circuit (that is, a data driver, thereafter being simply called a "driver") or a like, a digital image processing device can be applied to various display panels.

Figures 5A, 5B, and 5C are diagrams showing examples of methods for connecting various display panels to drivers in which

examples of arrangement of the drivers 501 each being made up of, for example, 96 pixels and being able to operate all image lines included in various display panels. If the driver 501 is commonly used for connecting display panels with different resolutions,

5   that is, the display panel 502 with WXGA resolutions, display panel 503 with HD resolutions, and display panel 504 with WVGA resolutions, in the case of the display panel 503 with HD resolutions, as shown in Fig. 5B, resolutions in a horizontal direction can be realized by fully using the driver 501 having

10   96 pixels. However, in the display panel 502 with WXGA resolutions and the display panel 504 with WVGA resolutions, as shown in Fig. 5A and Fig. 5C, unused pixels are left.

Moreover, the driver 501 is so constructed ordinarily that, in order to reduce the number of input terminals, after image data

15   has been captured from 2 to 4 pieces of input terminals in a time-series manner, 96 pixels are output in parallel (for example, uPD16341/A, 96-bit AC-PDP driver, Material number S14076JJ5V0PM00 (Fifth edition), June 1999).

Therefore, for example, in the case of the display panel

20   502 with WXGA resolutions and the display panel 504 with WVGA resolutions, it is necessary that data (hereafter, being referred as a "redundant pixel" or "dummy data") corresponding to portions being not connected between the display panel 502 or the display panel 504 and the driver 501 has to be embedded in an image line

25   to be transferred to the driver 501. Due to this, there are some cases in which a length of an image line to be transferred to a driver is longer than that to be actually displayed on a display panel. Moreover, a position in which dummy data is embedded and the number of pixels are varied depending on types of drivers.

In recent years, 192-bit and 256- bit drivers, besides 96-bit driver, are commercially available.

Figure 6 is a block diagram showing an example of configurations of a conventional digital image processing device. In a video input signal 601, after the video input signal 601 has been processed by a signal processing section 602, is embedded dummy data which corresponds to resolutions of a display panel to be used, by a redundant pixel embedding section 603. The image line in which dummy data is embedded, after having been stored in a frame memory 604, is transferred to each of drivers 605 in a time-series manner and is then displayed in a display panel 606 (with WXGA resolutions).

In a conventional image processing device, in order to transfer an image line containing dummy data which corresponds to a resolution of a display panel to a driver, in the case of, for example, a display panel with WXGA resolutions, as shown in Fig. 6, dummy data has been, in advance, embedded by the redundant pixel embedding section 603 in an output image line each having 4095 pixels in the signal processing section 602 so that the number of pixels becomes 4224 and the data having 4224 pixels is stored in the frame memory 604. Thus, by having the redundant pixel embedding section 603 embed dummy data corresponding to a resolution of a display panel, the digital image processing device can be applied to a display panel with a different resolution.

Moreover, so far as a research on prior art performed within a range of ordinary efforts is concerned, no information about references concretely describing contents of the above described conventional technology is obtained.

However, the conventional digital image processing device

has problems. That is, a first problem associated with the conventional digital image processing device is an increase in a capacity of a frame memory. This occurs because a redundant image line having embedded dummy data which is not actually displayed

5   is stored into a frame memory, that is, for example, if a display panel with WXGA resolutions uses a 96-bit driver, capacity being equivalent to about 3% of a total capacity of the frame memory is used for dummy data which is not displayed.

A second problem associated with the conventional digital

10 image processing is an increase in an amount of hardware. This occurs because both a function of embedding dummy data in an image line and a function of transferring data to a driver of a display panel in a time-series manner have to be individually designed.

15   SUMMARY OF THE INVENTION

In view of the above, it is an object of the present invention to provide a digital image processing device using a simplified circuit which is capable of eliminating waste in storing dummy

20 data in a frame memory and of being applied to a display panel employing a combination of a desired level of a resolution and any type of driver.

According to a first aspect of the present invention, there is provided a digital image processing device including:

25   a signal processing unit to process a video input signal;

a frame memory to store a result from the processing performed by the signal processing unit; and

a redundant pixel embedding circuit to embed a redundant pixel not to be displayed in an image line read from the frame

memory and to produce a video output signal.

In the foregoing, a preferable mode is one wherein the redundant pixel embedding circuit has a function of receiving, as an input, an image line read from the frame memory and of

5 embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image line.

Thus, in the digital image processing device of the present invention, dummy data is embedded not in data output from a signal

10 processing unit but in an image line read from the frame memory. Therefore, storing dummy data not to be displayed in the frame memory is not required.

According to a second aspect of the present invention, there is provided a digital image processing device including:

15   a signal processing unit to process a video input signal;

a frame memory to store a result from the processing performed by the signal processing unit;

a serial-parallel converting circuit to receive image data read from the frame memory in a time-series manner and to produce

20 an output making up an image line,

a redundant pixel embedding circuit to embed a redundant pixel not to be displayed in the image line and to output data, and

a parallel-serial converting circuit to output the image

25 line in which the redundant pixel is embedded as time-series image data.

In the foregoing, a preferable mode is one wherein the serial-parallel converting circuit which is made up of a register file being able to store an image line and which has a function

of sequentially storing image data fed from the frame memory in a time-series manner according to a writing control signal fed from outside and of reading, simultaneously and in parallel, contents of all registers in the register file.

5   Also, a preferable mode is one wherein the redundant pixel embedding circuit has a function of receiving, as an input, an image line read from the serial-parallel converting circuit and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in the image

10   line.

Also, a preferable mode is one wherein the parallel-serial converting circuit has a register file made up of two or more shift registers and a selector to select an output from each of the shift registers and to output the selected output and wherein the

15   register file is able to store an image line in one clock cycle and wherein each of the shift registers is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal and wherein the selector has a function of selecting a specified shift output from

20   the shift register and of outputting the selected output according to an embedding control signal fed from outside.

Furthermore, a preferable mode is one wherein each of the shift registers is made up of two or more split shift registers and wherein each of the split shift registers receives a data input,

25   shift data input, latch signal input, and shift signal input and produces a shift data output and wherein each of the shift registers has a function of writing, when data is to be written to the split shift registers, data at one time, by making active a latch signal input, in synchronization with a clock and, at time

of shifting operations, of performing the shifting operation for data, by making active a shift signal input, in synchronization with a clock and of feeding a shift output fed from each of the split shift registers to the selector by connecting a terminal for a shift output from each of the split shift registers to a terminal for a shift input of each of adjacent split shift registers to allow the shift register to perform the shift operation as a whole.

Thus, in the digital image processing device of the present invention, dummy data is embedded, in parallel, in an image line (one horizontal line) based on connection theory and the output is transferred, by using a shift register, to a data driver in a time-series manner. Therefore, both a function of embedding dummy data and a function of transferring data in a time-series manner to a driver of a display panel can be realized using simplified hardware and the present invention can be applied to a display panel having a combination of a desired level of resolution and any type of driver.

With the above configurations, it is made possible to decrease a required capacity of a frame memory and to reduce costs for components to be used as a frame memory and power consumption. This can be achieved because storing of dummy data not to be displayed in the frame memory is not required.

With another configuration, it is made possible to decrease an amount of hardware required in an output circuit for a data driver and to minimize a chip area (or costs) required when being incorporated in large-scale integrated circuits and to reduce power consumption. This can be achieved because both a function of embedding dummy data and a function of transferring data to

a driver of a display panel in a time-series manner can be realized using simplified hardware and the digital image processing device can be applied to a combination of a desired level of a resolution employed in the display panel and any type of driver employed in

5   the display panel.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages, and features of

10   the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing basic configurations of a digital image processing device according to one embodiment of

15   the present invention;

Fig. 2 is a diagram showing detailed configurations of a redundant image embedding section in the digital image processing device according to the embodiment of the present invention;

Fig. 3 is a diagram showing a concrete configuration example

20   of the redundant image embedding section in the digital image processing device according to the embodiment of the present invention;

Fig. 4 is a diagram showing a concrete configuration example of a parallel - serial converting circuit in the digital image

25   processing device according to the embodiment of the present invention;

Figs. 5A, 5B, and 5C are diagrams showing examples of methods for connecting various display panels and drivers; and

Fig. 6 is a block diagram showing an example of

configurations of a conventional digital image processing device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5   Best modes of carrying out the present invention will be described in further detail using various embodiments with reference to the accompanying drawings.

Embodiment

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Figure 1 is a block diagram showing basic configurations of a digital image processing device according to one embodiment of the present invention. Figure 2 is a diagram showing detailed configurations of a redundant image embedding section in the 15   digital image processing device according to the embodiment. Figure 3 is a diagram showing a concrete example of the redundant image embedding section in the digital image processing device according to the embodiment. Figure 4 is a diagram showing a concrete example of a parallel - serial converting circuit in the 20   digital image processing device according to the embodiment.

The digital image processing device of the embodiment chiefly includes, as shown in Fig. 1, a signal processing section 102, a frame memory 103, and a redundant pixel embedding section 104. The signal processing section 102, after having performed 25   processing of filtering, or a like, of a video input signal 101, outputs the filtered signal. The frame memory 103 holds image data for each frame. The redundant pixel embedding section 104, after having embedded dummy data in an image line input in a time-series manner, outputs the data as a video output signal 105.

Operations of the digital image processing device shown in Fig. 1 are described below. In the digital image processing device, a video input signal 101, after having been processed by the signal processing section 102, is stored in the frame memory 103 as image

5 data. The frame memory 103 is installed to play a role as a double buffer or a like to smooth out transfer speed discrepancies, for example, between the video input signal 101 and the video output signal 105. The video data read from the frame memory 103, after dummy data has been embedded in the video data by the redundant

10 pixel embedding section 104 and is fed to a display panel (not shown) as the video output signal 105.

The redundant pixel embedding section 104 in the digital image processing device of the embodiment, as shown in Fig. 2, is made up of a serial-parallel converting circuit 202, a

15 redundant pixel embedding circuit 203, and a parallel-serial converting circuit 204. The serial-parallel converting circuit 202, after having converted data input in a time-series manner from serial data to parallel data, outputs the converted data in a unit of an image line in parallel. The redundant pixel embedding

20 circuit 203 embeds dummy data in an image line and outputs the data. The parallel-serial converting circuit 204 parallel-serial converts an image line in which dummy data is embedded and produces a time-series video output signal.

Operations of the redundant pixel embedding section 104

25 shown in Fig. 2 are described below. In the redundant pixel embedding section 104, a frame memory output data 201 output in a time-series manner from the frame memory 103, after having undergone a serial-parallel conversion by the serial-parallel converting circuit 202, is output in a unit of an image line in

parallel. The redundant pixel embedding circuit 203 embeds dummy data in an input image line and outputs the data. The image line in which dummy data is embedded, after having undergone a parallel-serial conversion by the parallel-serial converting

5   circuit 204, is output as the video output signal 105 made up of time-series data.

Figure 3 is a diagram showing the concrete configuration example of the redundant image embedding section 104 in the digital image processing device according to the embodiment of

10   the present invention. To correspond to a display panel providing an image line with the maximum WXGA-type resolution, the redundant image embedding section 104 includes a register file 301 made up of sixty four pieces of 64-bit registers 307, a redundant pixel embedding circuit 303, a register file 305 made up of five pieces

15   of 768-bit shift registers 308a and of one piece of a 384-bit shift register 308b, and a selector 309.

Next, operations of the redundant pixel embedding section shown in Fig. 3 are described. The register file 301, according to a writing control signal 302, when sequentially capturing

20   64-bit data fed as frame memory output data 201 to the register 307 and then capturing an image line with the maximum WXGA resolution (4095 pixels / line), outputs all pixels making up an image line in parallel. In the case of an image line with the WXGA resolution or less, data is stored, for example, in a manner close

25   to the left relative to the register file 301 and a remainder is padded with 0s.

The redundant pixel embedding circuit 303 is constructed based on connection theory and, according to an embedding control signal 304, embeds dummy data in an input image line output from

the register file 307. The embedding control signal 304 is used to specify a position of dummy data to be embedded in the image line and may be a decoding signal to specify a resolution of a display panel, a type of driver (the number of pixels operated

5   by one driver), or a like.

The register file 305 captures image lines output from the redundant pixel embedding circuit 303 at a same time, for example, in five pieces of 768-bit shift registers 308a each containing 768 pixels and one piece of 384-bit shift register 308b containing

10   384 pixels, whose sum of the pixels is 4224 pixels, in synchronization with a clock in one cycle.

Moreover, the register file 305 performs a shift operation on the captured image line, according to a read control signal 306, in synchronization with a clock. While the shift operation

15   is being performed, the captured image line is output in a time-series manner from 5 pieces of 40-bit shift output terminals and from 1 piece of 20-bit shift output terminal. The selector 309 selects time-series data from the shifted outputs fed from the register file 305 according to an embedding control signal

20   304, and outputs the data as the video output data 105.

Figure 4 is a diagram showing a concrete configuration example of a parallel – serial converting circuit in the digital image processing device according to the embodiment of the present invention, and in detail, the shift register 308a made up of 96-bit

25   split shift registers 404, 64-bit split shift registers 405, and 32-bit split shift registers 406. Each of the 96-bit split shift registers 404 is made up of 4 pieces of 24-bit shift registers. Each of the 64-bit split shift registers 405 is made up of 4 pieces of 16-bit shift registers. Each of the 32-bit split shift

registers 406 is made up of 4 pieces of 8-bit shift registers. Each of the shifted outputs from the split shift registers is connected to each of shifted inputs from adjacent split shift registers, which make up 768-bit shift register as a whole.

5   The shift register 308a, by making a latch signal 402 active, captures redundant pixel embedding circuit output data 401 in one cycle in synchronization with a clock and performs a shifting operation, by making a shift signal 403 active, in synchronization with a clock. The split shift register 404 provides a shift length

10   of twenty-four bits and, therefore, input data is shifted out by twenty-four times shifting operations.

Similarly, the split shift register 405 provides a shit length of sixteen bits and, therefore, input data is shifted out by sixteen times shifting operations. The split shift register

15   406 provides a shift length of 8 bits and, therefore, input data is shifted out by 8 times shifting operations. Shift data of 4 bits is output from each of the split shift registers 404, 405, and 406 as an output corresponding to each of 96-bit, 192-bit and, 256-bit data drivers and is fed to a selector 309.

20   In Figs. 3 and 4, if an image line has a maximum WXGA resolution and corresponds to each of the 96-bit, 192-bit, and 256-bit data drivers, shift-out data output from the shift register 308a shown in Fig. 4 is input to the selector 309 shown in Fig. 3 which selects suitable shift-out data according to an

25   embedding control signal 304. However, the embedding control signal 304 has to contain a signal to specify a type of a driver, in addition to a signal to specify a resolution, both of which are required for embedding dummy data in the redundant pixel embedding circuit 303.

It is apparent that the present invention is not limited to the above embodiments but may be changed and modified without departing from the scope and spirit of the invention. For example, in the above embodiment, the digital image processing device of

5   the present invention is described in detail using a case of employing the WXGA resolution. However, the present invention may be applied not only to display panels with HD resolutions or WVGA resolutions being commercially available presently but also to display panels using a combination of a desired level of a

10   resolution employed in the display panel and any type of driver employed in the display panel being expected to appear in the market in future.